

IN THE CLAIMS

Please cancel claims 13-14.

Please amend the claims as follows.

- 1 1. (Currently Amended) An apparatus comprising:
 - 2 at least one processor;
 - 3 a memory coupled to the at least one processor;
 - 4 a partition manager residing in the memory and executed by the at least one
 - 5 processor, the partition manager managing allocation of a plurality of hardware resources
 - 6 to a plurality of logical partitions and managing communication between the plurality of
 - 7 logical partitions;
 - 8 an I/O adapter coupled to the at least one processor;
 - 9 a device driver for the I/O adapter, the device driver including an interface for
 - 10 performing an I/O operation on a first address of a first length by the I/O adapter, the
 - 11 device driver making a call to the partition manager passing the address of the first length
 - 12 to retrieve a corresponding address of a second length; and
 - 13 a memory tag mechanism that creates a memory tag of the first length that
 - 14 corresponds to a second address of the second length, wherein the memory tag comprises
 - 15 an identifier that ~~does not represent~~ cannot be mapped to a corresponding location in
 - 16 physical memory;
 - 17 wherein the partition manager, when the device driver makes the call to the
 - 18 partition manager passing the first address of the first length to retrieve the corresponding
 - 19 address of the second length, detects when the first address is a memory tag, and if so,
 - 20 returns the second address of the second length that corresponds to the memory tag.
- 1 2. (Original) The apparatus of claim 1 wherein the partition manager detects when the
- 2 first address is a memory tag by determining that the first address is in a predefined range
- 3 of addresses.

- 1 3. (Original) The apparatus of claim 1 wherein an address of the second length may be
2 used to initiate a redirected direct memory access operation by the memory tag
3 mechanism creating a memory tag of the first length that corresponds to the address of the
4 second length and passing the corresponding memory tag to the device driver.
- 1 4. (Original) The apparatus of claim 1 wherein the first length is 64 bits and the second
2 length is 32 bits.

- 1 5. (Currently Amended) A computer-implemented method for accessing a first logical
2 partition to access an I/O adapter allocated to a second logical partition, the method
3 comprising the steps of:
4 (A) creating a memory tag of a first length that corresponds to a second address of
5 a second length, wherein the memory tag comprises an identifier that ~~does not represent~~
6 cannot be mapped to a corresponding location in physical memory;
7 (B) passing the memory tag to a device driver for the I/O adapter;
8 (C) the device driver passing the memory tag to a partition manager to determine
9 the second address of the second length that corresponds to the memory tag, wherein the
10 partition manager manages allocation of a plurality of hardware resources to the first and
11 second logical partitions and manages communication between the first and second
12 logical partitions;
13 (D) the partition manager returning to the device driver the second address of the
14 second length that corresponds to the memory tag; and
15 (E) the device driver accessing the I/O adapter using the second address of the
16 second length that corresponds to the memory tag.
- 1 6. (Original) The method of claim 5 further comprising the step of the I/O adapter
2 performing a direct memory access (DMA) operation at a location specified by the second
3 address.
- 1 7. (Original) The method of claim 6 wherein the DMA operation comprises a redirected
2 DMA operation.
- 1 8. (Original) The method of claim 5 wherein step (D) comprises the step of the partition
2 manager detecting when the first address is a memory tag.

1 9. (Original) The method of claim 8 wherein the partition manager in step (D) detects
2 when the first address is a memory tag by determining that the first address is in a
3 predefined range of addresses.

1 10. (Original) The method of claim 5 wherein an address of the second length may be
2 used to initiate a redirected direct memory access operation by creating a memory tag of
3 the first length that corresponds to the address of the second length and passing the
4 corresponding memory tag to the device driver.

1 11. (Original) The method of claim 5 wherein the first length is 64 bits and the second
2 length is 32 bits.

1 12. (Currently Amended) A computer readable program product comprising:

2 (A) a memory tag mechanism that creates a memory tag of a first length that
3 corresponds to a second address of a second length, wherein the memory tag comprises
4 an identifier that ~~does not represent~~ cannot be mapped to a corresponding location in
5 physical memory, the memory tag being passed to a device driver for an I/O adapter, the
6 device driver including an interface for performing an I/O operation on a first address of a
7 first length by the I/O adapter, the device driver making a call to a partition manager
8 passing the address of the first length to retrieve a corresponding address of a second
9 length, the partition manager managing allocation of a plurality of hardware resources to
10 a plurality of logical partitions and managing communication between the plurality of
11 logical partitions, wherein the partition manager detects when the first address is a
12 memory tag, and if so, returns the second address of the second length that corresponds to
13 the memory tag; and

14 (B) ~~computer readable signal bearing~~ recordable media bearing the memory tag
15 mechanism.

1 13-14 (Cancelled)

1 15. (Original) The program product of claim 12 wherein the partition manager detects
2 when the first address is a memory tag by determining that the first address is in a
3 predefined range of addresses.

1 16. (Original) The program product of claim 12 wherein an address of the second length
2 may be used to initiate a redirected direct memory access operation by the memory tag
3 mechanism creating a memory tag of the first length that corresponds to the address of the
4 second length and passing the corresponding memory tag to the device driver.

1 17. (Original) The program product of claim 12 wherein the first length is 64 bits and the
2 second length is 32 bits.

Please add the following new claims

- 1 18. (New) An apparatus comprising:
2 at least one processor;
3 a memory coupled to the at least one processor;
4 a partition manager residing in the memory and executed by the at least one
5 processor, the partition manager managing communication between first and second
6 logical partitions;
7 an I/O adapter coupled to the at least one processor and allocated to the first
8 logical partition;
9 a first device driver for the I/O adapter residing in the first logical partition;
10 a memory tag mechanism residing in the first logical partition that creates a
11 memory tag of a first length that corresponds to a second address of a second length,
12 wherein the memory tag comprises an identifier that cannot be mapped to a
13 corresponding location in physical memory;
14 a second device driver for the I/O adapter residing in the second logical partition;
15 an application residing in the second logical partition that creates a buffer for
16 receiving data from the I/O adapter, the application performing a read operation to the
17 second device driver passing an address of the buffer;
18 in response to the read operation from the application, the second device driver
19 makes a call to the partition manager passing the address of the buffer, and in response
20 thereto, the partition manager returning a corresponding I/O address for the buffer;
21 the second device driver passing the I/O address for the buffer to the memory tag
22 mechanism, which generates therefrom a corresponding memory tag for the buffer that
23 cannot be mapped to a corresponding location in physical memory;
24 the memory tag mechanism making a call to the first device driver, passing the
25 memory tag for the buffer;
26 the first device driver, in response to the call by the memory tag mechanism,
27 making a call to the partition manager, passing the memory tag for the buffer;

28 the partition manager returning to the first device driver the I/O address of the
29 buffer;
30 the first device driver performing a read from the I/O adapter, passing the I/O
31 address of the buffer as a target location for the read; and
32 writing via direct memory access from the I/O adapter to the I/O address of the
33 buffer.

1 19. (New) A method for performing a direct memory access operation from an I/O
2 adapter in a first logical partition to an application in a second logical partition, the
3 method comprising the steps of:
4 the application creating a buffer for receiving data from the I/O adapter;
5 the application performing a read operation to a second device driver in the
6 second logical partition, passing an address of the buffer;
7 in response to the read operation from the application, the second device driver
8 making a call to a partition manager passing the address of the buffer;
9 in response to the call from the second device driver, the partition manager
10 returning a corresponding I/O address for the buffer;
11 the second device driver passing the I/O address for the buffer to a memory tag
12 mechanism, which generates therefrom a corresponding memory tag for the buffer that
13 cannot be mapped to a corresponding location in physical memory;
14 the memory tag mechanism making a call to the a device driver, passing the
15 memory tag for the buffer;
16 the first device driver, in response to the call by the memory tag mechanism,
17 making a call to the partition manager, passing the memory tag for the buffer;
18 the partition manager, in response to the call by the first device driver, returning to
19 the first device driver the I/O address of the buffer;
20 the first device driver performing a read from the I/O adapter, passing the I/O
21 address of the buffer as a target location for the read; and
22 writing via direct memory access from the I/O adapter to the I/O address of the
23 buffer.

1 20. (New) A computer readable program product comprising:
2 (A) a memory tag mechanism that creates a memory tag of a first length that
3 corresponds to a second address of a second length, wherein the memory tag comprises
4 an identifier that cannot be mapped to a corresponding location in physical memory,
5 wherein an application residing in a second logical partition creates a buffer for receiving
6 data from an I/O adapter residing in a first logical partition, the application performing a
7 read operation to a second device driver residing in the second logical partition passing an
8 address of the buffer, and in response to the read operation from the application, the
9 second device driver makes a call to a partition manager passing the address of the buffer,
10 and in response thereto, the partition manager returns a corresponding I/O address for the
11 buffer, the second device driver passing the I/O address for the buffer to the memory tag
12 mechanism in the first logical partition, the memory tag mechanism generating from the
13 I/O address for the buffer a corresponding memory tag for the buffer that cannot be
14 mapped to a corresponding location in physical memory, the memory tag mechanism
15 making a call to a first device driver in the first logical partition passing the memory tag
16 for the buffer, the first device driver, in response to the call by the memory tag
17 mechanism, making a call to the partition manager, passing the memory tag for the
18 buffer, the partition manager returning to the first device driver the I/O address of the
19 buffer, the first device driver performing a read from the I/O adapter, passing the I/O
20 address of the buffer as a target location for the read, and writing via direct memory
21 access from the I/O adapter to the I/O address of the buffer; and
22 (B) recordable media bearing the memory tag mechanism.